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REMARKS

This response is submitted in reply to the Final Office Action mailed January 27, 2006 ("the Action"). Claims 1-3, 5-20, 33, 34, 36-38, 44 and 45 are pending in this application. Claims 10-20, 33-35, 38, 44 and 45 are allowed. Claims 1-3, 5-9, 36 and 37 stand rejected as being obvious primarily based on the combination of primary reference U.S. Patent No. 5,459,345 to Okudaira et al. ("the '345 patent") in light of U.S. Patent No. 6,001,682 to Chien ("Chien").

Applicant respectfully requests reconsideration of the Action's claim rejections, including, *inter alia*, the characterization of the insulating layer 15 shown in Figure 15 of the '345 patent and the deficiencies of the new combination of the cited patent references.

The Action at ¶ 4, alleges that the combination of the cited patent references "anticipates" the subject matter of Claims 1-3, 5-9, 36 and 37. Applicant respectfully disagrees.

Claim 1 recites in-part, a lower electrode disposed on the oxidation barrier pattern, wherein the lower electrode has a cross-sectional shape that includes spaced apart extending parts defining an inner cavity portion with a closed bottom surface and an upper portion therebetween, wherein a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface area of the lower electrode.

The combination neither "anticipates" or renders the claimed subject matter obvious. Even if combined, the cited patents fail to disclose or suggest the claimed subject matter. The '345 patent proposes a barrier layer 11 that is formed by patterning a deposited layer 11 (*see* Figures 11 and 12, col. 16, lines 4-26) and a bottom electrode of the Chien patent is formed in an opening 309 that is formed by patterning an oxide layer 308 (*see* Figures 3D-3F, col. 2, lines 21-42). Therefore, if the barrier layer of the '345 patent and the bottom electrode of the Chien patent are combined, the combined structure requests an align margin region between the barrier layer of the '345 patent and the bottom electrode of the Chien patent. A top surface area of the barrier layer of the combined structure is NOT equal to a bottom surface area of the bottom electrode of the combined structure.

Applicant also respectfully reiterates that the capacitive insulating layer 15 of the '345 patent (which the Action calls the dielectric film 15) while covering the lower electrode 13 on

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three sides, is not conformal to the lower electrode sidewall 13 and the oxidation barrier sidewall, much less conformal to have a substantially straight line orientation over the lower electrode and barrier pattern sidewalls. The term "conformal" means at least has the general shape of or follows the shape of the underlying structure. Applicant submits that capacitive layer 15, as shown below for ease of reference, does not follow the shape of the lower electrode sidewall. Rather, if layer 15 follows a shape of anything, it follows the shape of the upper electrode. For example, referring to Figure 15, as layer 15 moves to the center of the figure, the layer 15 has an arcuate upper corner segment that merges into lower points and an arcuate center segment. This shape is not a straight line and more correctly stated corresponds to the shape of the upper electrode. In addition, unlike the claimed structure, the lower electrode 13 shown in Figure 15 has a planar upper surface, no cavity or straight sidewalls thereof is illustrated.

In addition, the capacitive insulating layer 15 of the '345 patent shown in Figure 15 appears to be relatively thick (having generally the same thickness as that of the lower electrode) which inhibits its ability to be "conformal" to the lower electrode or to have a straight line shape. Applicant invites the Examiner to "visually excise" layer 15 from Figure 15 to visualize the shape of the layer 15. In so doing, Applicant submits that the shape thereof is not the shape of the lower electrode sidewalls (and is not conformal thereto) and clearly does not have a straight-line configuration.

In contrast, see the claimed conformal structure shown in Figure 4 of the instant application.

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FIG. 15

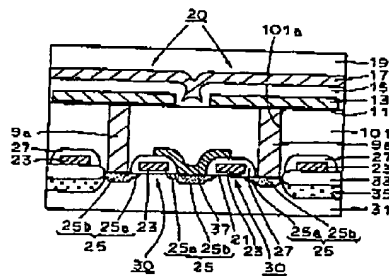
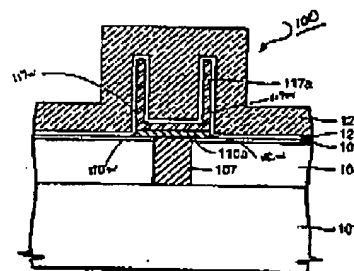


Fig. 4



Applicant submits that the '345 patent fails to teach or suggest at least the features emphasized below in Claims 1, 37 and 38.

1. (Previously Presented) A semiconductor device comprising:
 - an interlayer dielectric layer disposed on a semiconductor substrate;
 - a buried contact plug extending a distance through the interlayer dielectric to be in electrical communication with a predetermined region of the semiconductor substrate;
 - an oxidation barrier pattern disposed on a top surface of the buried contact plug;
 - a lower electrode disposed on the oxidation barrier pattern, wherein the lower electrode has a cross-sectional shape that includes spaced apart extending parts defining an inner cavity portion with a closed bottom surface and an upper portion therebetween, wherein a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface area of the lower electrode, wherein the lower electrode includes an external sidewall and the oxidation barrier pattern includes a sidewall, and wherein the lower electrode external sidewall and the oxidation barrier pattern sidewall are aligned in a substantially straight line; and
 - a dielectric film disposed over the lower electrode sidewalls, wherein the dielectric film conforms to the lower electrode sidewall and the oxidation barrier sidewall in a substantially straight line orientation.

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36. (Previously Presented) A semiconductor device according to Claim 1, wherein the lower electrode has a generally cylindrical shape with the closed bottom surface disposed on and coextensively with the oxidation barrier pattern, wherein the dielectric film defines a continuous surface between an upper electrode and the lower electrode and conformably resides against the surfaces defining the cavity of the lower electrode, and wherein a portion of the upper electrode fills the cavity of the lower electrode.

37. (Previously Presented) A semi-conductor device according to Claim 1, wherein, the spaced apart extending parts are configured as two substantially parallel spaced apart upwardly extending sidewalls.

Applicant respectfully submits that even combined the cited references fail to teach or suggest at least the emphasized features.

CONCLUSION

Applicant respectfully submits that the instant application is in condition for allowance, which action is requested. Applicant invites the Examiner to contact the undersigned for prompt resolution of any outstanding issues to expedite the allowance of the application.

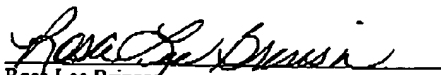
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Rosa Lee Brinson